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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,841	04/09/2004	Nobuo Karaki	119408	8476

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EXAMINER	
TAN, VIBOL	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 07/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/820,841	KARAKI, NOBUO
	Examiner	Art Unit
	Vibol Tan	2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 13-19* is/are rejected.

7)☒ Claim(s) *9-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/9/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: CSP method and LDD region are defined in the specification. Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 4, 5, 8, 14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mashiko (U. S. PAT. 6,034,563) in view of Eerenstein et al. (U. S. PAT. 5,097,151).

In claim 1, Mashiko teaches all claimed features in Figs. 9-18, a semiconductor integrated circuit, comprising: a plurality of circuit blocks (only one block of logic 11 shown) capable of transitions from an operating state (active state; col. 11, line 55) to a standby state (standby state; col. 11, line 57) and from a standby state to an operating state (inherent); and, a control circuit (12) which controls, in event-driven fashion, the back-gate voltages of transistors forming logic elements (TP1, TP3, TN1, TN2) of said circuit blocks; with the exception of teaching the control circuit which controls the back-gate voltages of the transistors, based on a finite state machine that stipulates in advance each of the state transitions of said plurality of circuit blocks. However,

Eerenstein et al in col. 1 that a finite-state machine is a frequently used model for representation of logic systems, and an FSM can be implemented in an FSM circuit.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to implement a finite state machine, as taught by Eerenstein et al., into the circuit of Mashiko, because transistors between states of the finite state machine are realized, such that the simulated circuit realizes the transition from an unknown state to a known state.

In claim 4, Mashiko further teaches the semiconductor integrated circuit according to Claim 1, further comprising: a common power supply line to supply power (VDD) to each of said plurality of circuit blocks; a common ground line to ground (ground) each of said plurality of circuit blocks; and switching elements (Q1, Q2) to perform electrical connection/disconnection between said circuit blocks (only one block of logic 11 shown) and at least either one of said common power supply line and said common ground line, wherein said control circuit (12) controls the connection/disconnection of said switching elements in an event-driven fashion, based on said finite state machine (Eerenstein et al.).

Claim 5 corresponds to detailed circuitry already discussed similarly with regard to claim 1.

Claim 8 corresponds to detailed circuitry already discussed similarly with regard to claim 4.

Claims 14 and 17 correspond to detailed circuitry already discussed similarly with regard to claim 1.

4. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mashiko in view of Eerenstein et al. as applied to claim 1 above, and further in view of Uvieghara (US 2004/0095176 A1).

In claim 13, Mashiko in view of Eerenstein et al. teaches the semiconductor integrated circuit according to Claim 1; with the exception of teaching electronic equipment comprising the semiconductor integrated circuit according to Claim 1. However, Uvieghara teaches in col. 1, the integrated circuit of claim 1 is employed in various demanding applications including personal computers, cell phones, watches, and finite state machines.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to employ the circuit of claim 1 in electronic equipment to minimize leakage current during sleep mode, so power is saved.

5. Claims 2-3, 6-7, 15-16 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mashiko in view of Eerenstein et al. as applied to claim 1 above, and further in view of JP A 9-83335.

In claim 2, Mashiko in view of Eerenstein et al. teaches the semiconductor integrated circuit according to Claim 1; with the exception of teaching wherein said control circuit controls said back-gate voltages such that, when said circuit blocks are in the standby state, the threshold voltages of said transistors are increased. However, JP A 9-83335 teaches a circuit block is in a standby state, the back-gate voltage is controlled such that the threshold voltage of the switching transistor rises, and the switching transistor is turned off.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to incorporate the teachings of Mashiko with the teachings of Eerenstein et al. and with the teaching of JP 9-83335, in order to decrease leakage currents (turn-off currents) in the standby state can, so that power consumption can be reduced.

In claim 3, JP A 9-83335 further teaches the semiconductor integrated circuit according to Claim 1, wherein said control circuit controls said back-gate voltages such that, when said circuit blocks are in the operating state, the threshold voltages of said transistors are decreased.

Claims 6 and 7 correspond to detailed circuitry already discussed similarly with regard to claims 2 and 3.

Claims 15 and 16 correspond to detailed circuitry already discussed similarly with regard to claims 2 and 3.

Claims 18 and 19 correspond to detailed circuitry already discussed similarly with regard to claims 2 and 3.

6. Claims 9-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VIBOL TAN
PRIMARY EXAMINER